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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,792	11/26/2003	David J. Corisis	MICS:0045-1 (FLE/MAN) 99	1002

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EXAMINER	
CAZAN, LIVIUS RADU	

ART UNIT	PAPER NUMBER
3729	

MAIL DATE	DELIVERY MODE
05/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/723,792	CORISIS, DAVID J.	
	Examiner	Art Unit	
	Livius R. Cazan	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-18 and 22-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-18 and 22-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. **Claims 16-18, 22, 24-31, and 33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Song (US5776799 to Song et al.) in view of Sim (US5840614 to Sim et al.).

Regarding claims 16-18, 22, 24-27, 29-31, and 33, as discussed in the rejection mailed on 12/28/2006, Song discloses substantially the same invention as the Applicant. Claims 16 and 26 have been amended to recite a step of grinding the wafer after producing the wafer map. Song discloses a step of back lapping the wafer to reduce its thickness (see col. 4, lns. 1-12).

However, it is not clear from the Song reference whether the grinding is performed prior to or after the EDS testing.

Sim discloses performing the grinding operation after having tested the die in an EDS process (see Fig. 4, steps 42 and 46).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to perform the grinding step after the EDS step, in order to reduce the risk of damage to the wafer. A thin wafer would be more likely to break during the handling of the wafer for testing purposes.

Regarding claim 28, the EDS process probed the die on the wafer to identify the working and non-working die. As disclosed by Song, during the EDS process ink dots

are used to mark defective die. The good die are thus marked by the absence of ink dots. The wafer itself therefore constitutes a map of good and bad die.

3. **Claims 23 and 32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Song and Sim in view of Jiang (US6524891).

Song and Sim disclose the same invention as the applicant, except for the circuit package being a board-on-chip (BOC) package.

It is readily apparent to anyone skilled in the art that the process of Song and Sim focuses on applying adhesive to the IC die on the substrate. Therefore the choice of packaging technology is purely a design consideration. Jiang teaches the manufacturing of both LOC and BOC packages (see Figs. 3 and 1 respectively), in both cases adhesive strips (10, 10B, Figs. 1 and 3) being utilized to bond the die to the leadframe or substrate.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the process of Song and Sim to form a BOC circuit package, since the BOC package is an art recognized equivalent package structure.

Response to Arguments

4. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues (page 7) the examiner has misinterpreted the recitation of a "wafer map", since the wafer map is utilized after the wafer surface is modified, and therefore the ink markings would not constitute a map. Applicant further argues the Song reference does not teach *grinding the wafer map or identifying the electrically*

good circuit die, and that if Song did teach a grinding step, the ink would be ground away before it could be utilized to determine which die should receive adhesive.

The examiner respectfully disagrees. It would appear Applicant has misinterpreted the recitation "the integrated circuit wafer is ground to a desired thickness" (page 12, lns. 12-22 of the present specification). As currently described din the specification, one of skill in the art is led to believe the grinding step refers to grinding the back of the wafer to reduce the thickness of the wafer (i.e. back lapping), as is very well known in the art and as is disclosed by Song (see the rejection above). It would appear Applicant interpreted this grinding step as a step of grinding the surface of the wafer, i.e. the circuits.

Since the back lapping process removes material from the back of the wafer, the circuitry and the ink dots are not affected, and the ink dots can be used to selectively apply adhesive to the die, as disclosed by Song. Further, Song *does* disclose identifying the electrically-good circuit die. Applicant agrees (see bottom of page 7) that in the Song reference defective chips on the wafer are identified with ink dots during EDS and that adhesive is only deposited on non-defective functional chips. Clearly, this constitutes identifying the electrically-good circuit die. How else can the defective die be identified if not by probing the die to determine which die operate properly and which do not? Moreover, the die having ink dots deposited thereon *do* constitute a wafer map, because they allow the adhesive-applying means to distinguish between working and non-working die. As currently claimed the map does not have to take a specific form,

such as an image on a computer screen, or on a sheet of paper, but can be anything that identifies the good die from the bad.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

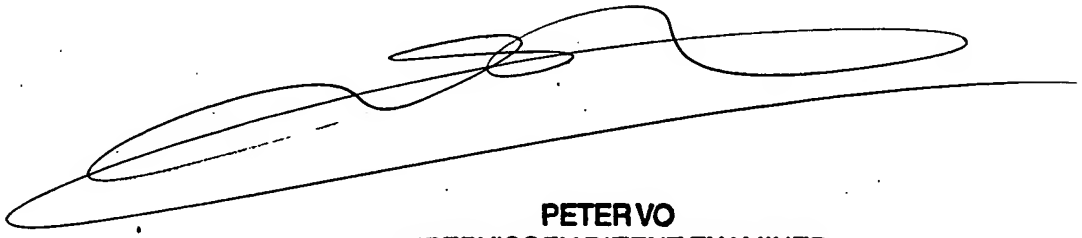
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Livius R. Cazan whose telephone number is (571) 272-8032. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on (571)272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LRC 04/30/2007



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